storing at least a portion of the data in a register communicably coupled to a bus, the bus including at least one data line for transmitting the data, and at least one clock line for transmitting a clock signal at a first clock rate and at a second clock rate less than the first clock rate, the storing step including storing the at least a portion of the data in the register while the clock signal is being transmitted at least at the second clock rate; and

driving the clock line to a low logic level while the data is stored in the register.

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REMARKS

The instant Amendment is filed in response to the official action dated September 17, 2002. Reconsideration is respectfully requested.

Claims 1-9 are currently pending.

Claims 1-9 stand rejected.

Claims 1 and 6 have been amended to more distinctly claim the Applicants' invention.

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The Examiner has rejected base claims 1 and 6, and dependent claims 2, 5, and 7, under 35 U.S.C. 103(a) as being unpatentable over Trieu et al. (USP 5,925,135) in view of Carson et al. (USP 5,920,156). The Examiner has further rejected dependent claims 3-4 and 8-9 under 35 U.S.C. 103(a) as being unpatentable over Trieu et al. in view of Carson et al. as applied to claims 1 and 6, and further in view of Hamilton et al. (USP 4,443,845). However, the Applicants respectfully submit that the official action fails to establish a *prima facie* case of obviousness.

It is well settled that a *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art. The mere fact that the prior art may be combined in the manner suggested in the official action neither makes the combination *prima facie* obvious nor obvious unless the prior art suggests the desirability of the combination. Because none of the cited references taken alone suggests the claimed subject matter, and because the cited references themselves fail to suggest any desirability of combining them, the rejections of claims 1-9 under 35 U.S.C. 103(a) cannot be sustained.

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Specifically, the Applicants' claimed system and method solves the problem of performing data transfer operations via a bus such as an SMBus by a computer, whether or not the computer is "sleeping" (*i.e.*, operating in a reduced frequency or suspended power state). Such data transfers are accomplished by providing a register communicably coupled to the bus for storing at least a portion of the data carried by the bus, and a pull-down switch for extending the low period of a clock signal to synchronize the data transfer operation with the speeds of devices involved in the data transfer (see page 4, line 26, to page 5, line 6, of the application).

The Trieu reference addresses the problem of interfacing a low frequency device to a bus such as the SMBus having at least one other device operating at a higher frequency (see column 1, lines 5-10, and lines 31-33, of Trieu et al.). Moreover, the Carson reference addresses the problem of conveying dimmer station address signals via a lighting control/dimming system independently of line phase per dimmer station or controller station (see column 2, lines 46-50, of Carson et al.).

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The Applicants respectfully submit that the problem addressed by the Carson reference has no bearing on the nature of the problem solved by the Applicants' system and method. For example, the problem solved by the claimed system and method arises from the operational characteristics of a computer executing power management functions. Such a computer may be operative at a first clock rate when it is "awake" (*i.e.*, operating at its normal operating frequency and power state), and may be operative at a second reduced clock rate when it is sleeping. The Applicants' system and method enables the computer to successfully transfer data over a bus such as the SMBus whether or not the computer is in the awake or sleep mode of operation.

In contrast, the Carson reference allows control signals to be sent from a controller to a plurality of dimmer switch stations independently of the line phase of power supplying each dimmer or controller (see column 4, lines 47-57, of Carson et al.). The Carson reference has nothing to do with transmitting data between devices operating at different frequencies, nor is it concerned with data transmission between devices over a bus such as the SMBus, nor does it address problems relating to computerized devices executing power management functions.

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Because there is no teaching in the Trieu and/or Carson references to combine the prior art references as suggested in the official action, one of ordinary skill in the art would have no motivation to make the suggested combination. Accordingly, the Applicants respectfully submit that a *prima facie* case has not been established, and therefore the rejections of the base claims 1 and 6 and the claims dependent therefrom under 35 U.S.C. 103(a) are unwarranted and should be withdrawn.

Even if a *prima facie* case of obviousness were established, the suggested combination of the Trieu and Carson references would not render amended base claims 1 and 6 obvious. Specifically, the official action indicates that the Trieu reference does not teach the first device operative at least at the second clock rate to store at least a portion of the data in a register, and the second device operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device, as recited in amended base claims 1 and 6. The official action further indicates that the Carson reference teaches "operative at least at the second clock rate to store at least a portion of the data in a register (specification,

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column 5, line 61, to column 6, line 6), and operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device (specification, column 8, lines 9-13)."

However, the Applicants respectfully submit that the Carson reference fails to disclose the operation of driving the clock line to a low logic level while the data is stored in the register, as recited in amended claims 1 and 6. For example, the passage cited in the official action (*i.e.*, column 8, lines 9+, of Carson et al.) discloses, in relevant part, that each time a zero crossing signal makes a high to low transition, such as shown by the down directed arrows in Fig. 8 of the Carson reference, the remote input to the micro-controller is sampled to obtain the logic level. This passage further discloses that if the remote input is high, then the LSB for one remote input register is set to logic "1" - if the remote input is low when the zero crossing makes its high to low transition, then *the LSB of the register* is cleared to a "0".

The register **64**, as described above and disclosed in the Carson reference, does not function as a clock line, but instead

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functions as a shift register to hold the bits of a HEX encoded data word received over the remote input, for subsequent comparison with bits stored in a serial encoder register **70** (see column 6, lines 54+, and Fig. 3, of Carson et al.). Clearly, the LSB of the register **64** reset to a "0" cannot correspond to the clock line driven to a low logic level, as recited in amended claims 1 and 6. Moreover, the Trieu and Hamilton references fail to cure this deficiency of the Carson reference. The Applicants therefore submit that even if the Trieu, Carson, and Hamilton references were combined in the manner suggested in the official action, the resulting combination would not meet amended base claims 1 and 6, and thus neither Trieu, Carson, nor Hamilton taken alone, nor any combination thereof, can render amended base claims 1 and 6 and the claims dependent therefrom obvious. Accordingly, the Applicants respectfully submit that the rejections of claims 1-9 under 35 U.S.C. 103(a) are unwarranted and should be withdrawn.

In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

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Application No. 09/591,044
Filed: June 9, 2000
Group Art Unit: 2181

The Examiner is encouraged to telephone the undersigned attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

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MARKED-UP VERSION OF CLAIM AMENDMENTS

1. (Amended) A system for transferring data between a plurality of devices [communicably coupled to a bus, the bus including at least one data line for transmitting the data and at least one clock line, the system], comprising:

a bus including at least one data line for transmitting the data and at least one clock line;

[the system being operative at a first clock rate and at a second clock rate less than the first clock rate;]

a first device communicably coupled to the bus [and operative at least at the second clock rate to store at least a portion of the data in a register]; and

a second device communicably coupled to the bus [and operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device],

wherein the system is operative at a first clock rate and at a second clock rate less than the first clock rate,

wherein the first device is operative at least at the second clock rate to receive at least a portion of the data transmitted over the data line, and to store the at least a portion of the data in a register, and

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wherein the second device is operative at least at the second clock rate to drive the clock line to a low logic level while the data is stored in the register of the first device.

6. (Amended) A method [for] of transferring data between a plurality of devices [communicably coupled to a bus, the bus including at least one data line for transmitting the data and at least one clock line for transmitting a clock signal at a first clock rate and at a second clock rate less than the first clock rate, the method], comprising the steps of:

[while the clock signal is being transmitted at least at the second clock rate,] storing at least a portion of the data in a register communicably coupled to [the] a bus, the bus including at least one data line for transmitting the data, and at least one clock line for transmitting a clock signal at a first clock rate and at a second clock rate less than the first clock rate, the storing step including storing the at least a portion of the data in the register while the clock signal is being transmitted at least at the second clock rate; and

driving the clock line to a low logic level while the data is stored in the register.

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